FORM PTO-1390
REV. 5-93

US DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEYS DOCKET NUMBER
P99,0886

U.S.APPLICATION NO. (if known, see 37 CFR 1.5)
09/308478

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/DE97/02600	**November 11, 1997**	**November 18, 1996**

TITLE OF INVENTION **COMPUTER-SUPPORTED METHOD FOR PARTITIONING AN ELECTRICAL CIRCUIT**

APPLICANT(S) FOR DO/EO/US **UTZ WEBER and GINGHUS ZHENG**

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay.
4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of International Application (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2).

7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. §371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)) **(attached at back of English translation of application)**.

9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98; **(PTO 1449, Prior Art, Search Report)**.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included.
    (SEE ATTACHED ENVELOPE)

13. ☒ A FIRST preliminary amendment.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ A change of power of attorney and/or address letter.

16. ☒ Other items or information:
    a. ☒ Submission of Drawings
    b. ☐ Letter Under Rule Under 37 C.F.R. §1.41(c)
    c. ☒ EXPRESS MAIL #EL294310959US

U.S.APPLICATION NO. (if known, see 37 C.F.R. 1.5)	INTERNATIONAL APPLICATION NO. PCT/DE97/02600	ATTORNEY'S DOCKET NUMBER P99,0886

17. ☒ The following fees are submitted:

	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5): Search Report has been prepared by the EPO or JPO ..... ~~$970.00~~ 840.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) ... $760.00		
No international preliminary examination fee paid to USPTO (37 C.F.R. 1.482) but international search fee paid to USPTO (37 C.F.R. 1.445(a)(2) $450.00		
Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2) paid to USPTO $1,250.00		
International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) ..... $ 98.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ ~~970.00~~ 840.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	9 - 20 =		X $ 22.00	$	
Independent Claims	1 - 3 =		X $ 82.00	$	
Multiple Dependent Claims			$270.00 +	$	
TOTAL OF ABOVE CALCULATIONS =				$ ~~970.00~~ 840.00	
Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 C.F.R. 1.9, 1.27, 1.28)				$	
SUBTOTAL =				~~$ 970.00~~ 840.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
TOTAL NATIONAL FEE =				$	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). $40.00 per property +				**SEE ATTACHED ENVELOPE**	
TOTAL FEES ENCLOSED =				~~$ 970.00~~ 840.00	
				Amount to be refunded	$
840.00				charged	$

a. ☒ A check in the amount of $ ~~970.00~~ to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **08-2290**. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Hill, Steadman & Simpson
A Professional Corporation
85th Floor Sears Tower
Chicago, Illinois 60606

Steven H. Noll
SIGNATURE

Steven H. Noll
NAME

28,982
Registration Number

BOX PCT

IN THE UNITED STATES ELECTED OFFICE
OF THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY - CHAPTER II

APPLICANT:	Utz Wever, et al.	ATTORNEY DOCKET NO. P99,0886
SERIAL NO.		GROUP ART UNIT:
FILING DATE:		EXAMINER:

INTERNATIONAL APPLICATION NO. PCT/DE97/02600

INTERNATIONAL FILING DATE: November 7, 1997

INVENTION: "COMPUTER-SUPPORTED METHOD FOR PARTITIONING AN ELECTRICAL CIRCUIT"

PRELIMINARY AMENDMENT

To: Assistant Commissioner of Patents
Washington, D.C. 20231

S I R:

Amend the above-identified international application before entry into the national stage before the U.S. Patent and Trademark Office under 35 U.S.C. §371 as follows:

IN THE SPECIFICATION

At page 1, line 1, insert the title --TITLE--.

At page 1, line 4, insert the heading --BACKGROUND OF THE INVENTION--.

At page 1, line 4 after the title, insert the following paragraph:

--The present invention relates to computer-implemented systems for simulating electronic or electrical circuits.--

At page 1, line 18, change "It is" to --First, it is--.

At page 1, line 24, change "Further" to --Second--.

At page 2, line 1, after "for" insert --the--.

At page 2, line 2, change "known from document [1] as" to --the--.

At page 2, line 3, after "SPICE." insert --See I. Hoefer, et al., *SPICE Analyseprogramm fur electronische Schaltungen*, Springer, Berlin (1985), pp. 7-22.--

At page 2, line 4, change "Documents [2] and [3]" to --U. Kleis, et al., *Doman Decomposition Methods for Circuit Simulation*, Proceedings of the 8th Workshop on Parallel and Distributed Simulation, PADS, Edinburgh, UK (July, 1994), pp. 183-86, and U. Wever, et al., *Parallel Transient Analysis for Circuit Simulation*, Proceedings of the 29th Annual Hawaii International Conference on System Sciences (1946), pp. 442-47--.

At page 2, line 8, change "Document [4]" to --B. Riess, *Partitioning Very Large Circuits Using Analytical Placement Techniques*, Proceedings of the 31st ACM/IEEE Design Automation Conference (1994), pp. 646-51--.

At page 2, line 21, change "[5]" to --P. Johannes, *Partitioning of VLSI Circuits and Systems*, 33rd Design and Automation Conference, Las Vegas (June 3-7, 1996), pp. 83-87--.

At page 2, line 23, change "[6]" to --J. Cong, et al., *A Parallel Bottom-Up Clustering Algorithm with Applications to Circuit Partitioning in VLSI Design*, 30th ACM/IEEE Design Automation Conference, June 14-18, 1993, pp. 755-760--.

At page 2, line 24, insert the following title:

--SUMMARY OF THE INVENTION--

At page 2, line 24, after inserting the above title, change "The method [sic] is thus based on the problem of specifying" to --The present invention provides--.

At page 2, line 27, delete the sentence "The problem is solved by the method accordin to patent claim 1." and insert the following paragraph:

--To that end, in an embodiment the invention provides a computer-supported method for partitioning an electrical circuit,

- whereby the electrical circuit is imaged onto a graph that exhibits the same topology as the electrical circuit,

- whereby edges of the graph have weighting values allocated to them with which a required calculating outlay for determining electrical descriptive quantities for elements of the electrical circuit that are represented by the respective edge is described,

- whereby a first sum value of the weighting values of the edges is calculated for edges coupled to one another and, in further iterations, the first sum value is respectively formed upon addition of at least one further edge until the respectively calculated, first sum value is greater than a prescribable, first threshold,

- whereby a partition of the electrical circuit is formed by the edges taken into consideration in the formation of the first sum value,

- whereby the following steps are implemented for at least a part of the remaining edges that do not lie in the partition and that are coupled to at least one edge of the partition:

- a second sum value is determined that derives from the sum of the first sum value and at least one weighting value of at least one remaining edge,

- when the second sum value is smaller than a prescribable second threshold, and

- when a plurality of edges that were taken into consideration in the formation of the second sum value that are coupled to edges that were not taken into consideration in the formation of the second sum value is smaller than a plurality of edges of the partition that are coupled to the remaining edges, then

- the remaining edge is allocated to the partition and the second sum value is allocated to the first sum value, and

- whereby the partition is formed by the edges taken into consideration in the formation of the second sum value.--

At page 3, line 12, change "document [4]" to --B. Riess in *Partitioning Very Large Circuits Using Analytical Placement Techniques*, Proceedings of the 31st ACM/IEEE Design Automation Conference (1994) pp. 646-651.--

At page 3, line 15, change "upon employment of" to --employing--.

At page 3, line 16, delete "inventively"; same line, after "determined" insert --in accordance with the invention--.

At page 4, lines 3-4, delete "Advantageous developments of the invention derive from the dependent claims." and insert the following:

--In an embodiment of the invention, at the beginning of the method, a grouping of elements of the electrical circuit is executed for which it is respectively found that these elements are allocated in common to a partition.

In an embodiment of the invention, at least one of the following rules is applied in the grouping of the elements of the electrical circuit:

- elements of a controlled source, at least one controlling element, and the controlled source are allocated in common to a partition,

- connecting loops in the electrical circuit that only contain at least one voltage source and at least one counter-inductance are allocated in common to a partition,

- no shorts dare arise due to the partitioning.

In an embodiment of the invention, a plurality of edges of the graph have a common weighting value allocated to them.

In an embodiment of the invention, the graph of the partition is mapped onto the electrical circuit, whereby the partition comprises the elements of the electrical circuit corresponding to the implemented partitioning.

In an embodiment of the invention, the method comprises the steps of iterating the method a plurality of times thereby forming a plurality of partitions, and determining electrical descriptive quantities for the elements of the electrical circuit for each partition, at least a part of the partitions being processed in parallel on a plurality of computers and/or processors.

In an embodiment of the invention, the parallel processing of the partitions is centrally controlled.

In an embodiment of the invention, at least a part of the partitions is centrally controlled in such a way that all terminals of the respective partition are coupled only to a central control unit, and a communication of data ensues only between the central control unit and at least the part of the partitions.

In an embodiment of the invention, a voltage source is additionally allocated at least to a part of the terminals of the respective partition, the value of said additional voltage predetermined by the central control unit during the determination of the electrical descriptive quantities.

In an embodiment of the invention, a resistor is additionally allocated at least to a part of the terminals of the partition.

At page 4, lines 22-24, delete "The Figures show an exemplary embodiment of the method that is explained in greater detail below. Shown are:" and insert the following paragraph:

--These and other features and aspects of the invention will become clear in the following detailed description of a few typical exemplary embodiments with reference to the accompanying drawings.--

At page 4, line 24, insert the title:

--BRIEF DESCRIPTION OF THE DRAWINGS--.

At page 4, line 25, after "Fig. 1" insert --is--.

At page 4, line 26, after "Fig. 2" insert --is--.

At page 4, line 27, insert the following heading:

--DETAILED DESCRIPTION OF THE
PRESENTLY PREFERRED EMBODIMENTS—

At page 4, line 28, change "Electrical" to --In accordance with the invention, electrical--.

At page 5, line 10, change "the document [1]" to --L. Hoefer, et al. in *SPICE Analyseprogramm for electronische Schaltungen*, Springer, Berlin (1985), pp. 7-22.--

At page 5, line 14, change "In" to --With reference now to the figures, in--; same line, change "on" to --onto--.

At page 6, line 19, change "is basically uncritical" to --basically is not critical--.

At page 6, line 21, change "A n" to --An--.

At page 7, line 23, after "steps" insert --designated 108--.

At page 7, line 24, after "implemented" delete "108".

At page 7, line 29, after "formed" insert --at--.

At page 8, line 3, after "Si" insert --at--.

At page 8, line 11, after "added" insert --at--.

At page 8, line 18, after "coupled" insert --at--.

At page 8, line 22, change "described later [sic]" to --(described later)".

At page 8, line 26, after "added" insert --at--.

At page 8, line 28, after "added" insert --at--.

At page 9, line 7, after "employed" insert --at--.

At page 9, line 14, after "back-imaging" insert --at--.

At page 10, line 26, insert the following paragraph:

--Although modifications and changes may be suggested by those skilled in the art, it is the intention of the inventors to embody within the patent warranted hereon all changes and modifications as reasonably and properly come within the scope of their contribution to the art.--

At page 12, line 1, change "Patent Claims" to --WHAT IS CLAIMED IS:--.

IN THE CLAIMS

Please amend the claims as follows:

1. (Amended) A [Computer] computer-supported method for partitioning an electrical circuit comprising the steps of:[,]

- [whereby] imaging the electrical circuit is imaged onto a graph that exhibits the same topology as the electrical circuit[,];

- [whereby] allocating weighting values to edges of the graph [have weighting values allocated to them] with which a required calculating outlay for determining electrical descriptive quantities for elements of the electrical circuit that are represented by the respective edge is described[,];

- [whereby] a first sum value of the weighting values of the edges [is calculated] for edges coupled to one another and, in further iterations, the first sum value is respectively formed upon addition of at least one further edge until the respectively calculated, first sum value is greater than a [prescribable] prescribable, first threshold[,];

- [whereby] forming a partition of the electrical circuit [is formed] by the edges taken into consideration in the formation of the first sum value[,];

- [whereby the following steps are implemented] for at least a part of the remaining edges that do not lie in the partition and that are coupled to at least one edge of the partition[:];

- determining a second sum value [is determined] that derives from the sum of the first sum value and at least one weighting value of at least one remaining edge[,];

- when the second sum value is smaller than a prescribable second threshold, and [--]when a plurality of edges that were taken into consideration in the formation of the second sum value that are coupled to edges that were not taken into consideration in the formation of the second sum value is smaller than a plurality of edges of the partition that are coupled to the remaining edges, then

- allocating the remaining edge [is allocated] to the partition and allocating the second sum value [is allocated] to the first sum value, and

- [whereby] forming the partition [is formed] by the edges taken into consideration in the formation of the second sum value.

2. (Amended) [Method] The method according to claim 1, [whereby a] wherein, at the beginning of the method, grouping of elements of the electrical circuit for which it is respectively found that these elements are allocated in common to a partition [is implemented at the beginning of the method].

3. (Amended) [Method] The method according to claim 2, [whereby] wherein at least one of the following rules is applied in the grouping of the elements of the electrical circuit:

- elements of a controlled source, at least a controlling element and the controlled source, are allocated in common to a partition,

- connecting loops in the electrical circuit that only contain at least one voltage source and at least one counter-inductance are allocated in common to a partition,

- no shorts dare arise due to the partitioning.

4. (Amended) [Method] The method according to [one of the claims 1 through 3, whereby] claim 1, wherein a plurality of edges of the graph have a common weighting value allocated to them.

5. (Amended) [Method] The method according to [one of the claims 1 through 4, whereby] claim 1, wherein the graph of the partition is imaged onto the electrical circuit, whereby the partition comprises the elements of the electrical circuit corresponding to the implemented partitioning.

6. (Amended) [Method] The method according to [one of the claims 1 through 5] claim 1, comprising the further steps of:

- [whereby] iterating the method a plurality of times thereby forming a plurality of partitions [are formed by multiple implementation of the method], and

- [whereby the] determining electrical descriptive quantities for the elements of the electrical circuit [are determined] for each partition, [whereby] at least a part of the partitions [is] being processed in parallel on the plurality of computers and/or processors.

7. (Amended) [Method] The method according to claim 6, [whereby] wherein the parallel processing of the partitions is centrally controlled.

8. (Amended) [Method] The method according to claim 7, [whereby] wherein at least a part of the partitions are centrally controlled in such a way that all terminals of the respective partition are coupled only to a central control unit and[, thus,] a communication of data ensues only between the central control unit and at least the part of the partitions.

9. (Amended) [Method] The method according to claim 8, [whereby] a voltage source is additionally allocated at least to a part of the terminals of the respective partition, the value of said additional voltage source [to be] predetermined by the central control unit during the determination of the electrical descriptive quantities.

10. (Amended) [Method] The method according to claim 9, [whereby] wherein a resistor is additionally allocated at least to a part of the terminals of the respective partition.

IN THE ABSTRACT OF THE DISCLOSURE

At page 15, line 1, change "ABSTRACT" to --ABSTRACT OF THE DISCLOSURE--.

At page 15, line 2, delete "Computer-Supported Method for Partitioning an Electrical Circuit".

Please amend the Abstract of the Disclosure to read as follows:

--A partition of an electrical circuit is formed in that the electrical circuit is imaged on a graph (102) and weighting values are allocated (103) to the edges of the graph. The weighting values describe a required calculating outlay for determining electrical descriptive quantities for the respective element of the electrical circuit represented by the edge. A check

is carried in iterative methods to see whether, proceeding from preceding iteration steps, [edges grouped together [sic],] [...] a sum of the weighting values of [the] edges grouped together [[...] a sum value] lies between a first threshold and a second threshold by adding a further edge. When this is the case, then a further check is carried out to see whether a plurality of terminals of the elements within the partition to elements outside the partition is increased by adding new edges. When this is not the case, then the respective edge is also incorporated into the partition.

REMARKS

The foregoing amendments to the specification and claims under Article 41 of the Patent Cooperation Treaty place the application into a form for prosecution before the U.S. Patent and Trademark Office under 35 U.S.C. §371 by reorganizing certain passages, correcting idiomatically incorrect passages and conforming the specification and claims. It is believed that no new matter has been entered. Accordingly, entry of these amendments before examination on the merits is hereby requested.

Respectfully submitted,

Steven H. Noll, Reg. No. 28,982

Steven H. Noll
HILL & SIMPSON
A Professional Corporation
85th Floor - Sears Tower
Chicago, Illinois 60606
Telephone (312) 876-0200

Attorneys for Applicant

SPECIFICATION

COMPUTER-SUPPORTED METHOD FOR PARTITIONING AN ELECTRICAL CIRCUIT

In circuit simulation of very large circuits, i.e. of circuits having a great plurality of elements, a serial processing, i.e. the determination of the circuit quantities by a computer, is extremely time-consuming. Even vector computers that are very expensive in terms of operation have an immense need of calculating capacity and time for determining the electrical descriptive quantities for a circuit that comprises a few 100,000 transistors.

In order to avoid the serial implementation of a circuit simulation for this reason, the electrical circuit can be divided into a plurality of parts that are then respectively processed by different computers or, respectively, processors, this leading to a parallel implementation of the circuit simulation.

In order, however, to achieve an optimally good parallelization of the determination of the electrical descriptive quantities for the electric circuit, it is advantageous to consider the following two criteria in the partitioning of the electrical circuit into a plurality of parts. It is of considerable significance that all partitions of the electrical circuit that are formed are of the same size insofar as possible, in order to thereby intensify the effect that can be achieved by the parallelization. When, for example, one partition is orders of magnitude larger than the remaining partitions, then the processing of the significantly larger partition is in turn far more calculation-consuming then the processing of the remaining partitions. Further, it is important in the partitioning that only a slight plurality of connections exists between the individual partitions insofar as possible since, in known methods for "parallelized" circuit simulation, the required transmission capacity, i.e. the required communication between the computers or, respectively, processors that respectively process one partition, increases substantially with an increasing number of existing connections between the partitions.

A language for textual description of an electrical circuit that can be processed by a computer is known from document [1] as circuit simulation language SPICE.

Documents [2] and [3] describe how a parallelized circuit simulation can be implemented, assuming an arbitrary number of partitions of the electrical circuit exist. The way in which the partitions can be determined is not described in these documents.

Document [4] discloses a global partitioning method on what is referred to as the logic level, which is also referred to as gate level.

Discrete events are described on the logic level, but no steady dynamic property of an electrical circuit on what is referred to as the transistor level, i.e. on the actual physical level of the electrical circuit, can be described with these.

The results of a circuit simulation that ensues on the logic level is thus unreliable and imprecise for certain applications since an exact time course of the electrical signals that occur in the electrical circuit cannot be taken into consideration.

Further, a description of the individual gates is required for the circuit simulation, this having to be determined first before the method can be implemented.

An overview of various partitioning rules can be found in [5].

A parallelized method for clustering an electrical circuit according to what is referred to as the bottom-up principle is disclosed by [6].

The method [sic] is thus based on the problem of specifying a method for partitioning an electrical circuit that directly considers the elements of the electrical circuit on the transistor level.

The problem is solved by the method according to patent claim 1.

In the method, the electrical circuit is imaged onto a graph that exhibits the same topology as the electrical circuit. The edges of the graph are weighted with weighting values that describe in approximately required calculating outlay for determining electrical descriptive quantities for the element of the electrical circuit respectively represented by the edge. A

partition for the electrical circuit is formed in the graph in that edges coupled with one another are combined to form the partition at the beginning of the method until the sum of the weighting values of the combined edges is greater than a first, prescribable threshold. When the first threshold is reached, the partition is then respectively expanded by further, remaining edges when the sum of the weighting values of all edges, including the edges to be potentially newly added, is smaller than a prescribable, second threshold, and when the plurality of edges of the partition that are connected to nodes that do not lie within the partition is reduced by the addition of at least one new edge.

The method exhibits a number of substantial advantages compared to the method disclosed by document [4].

Since the method works directly of the transistor level of the electrical circuit, the results achieved by the method are substantially more exact and dependable given a later circuit simulation upon employment of the partitions that have been inventively determined.

Advantageous developments of the invention derive from the dependent claims.

For prescribable elements of the electrical circuit, it is advantageous to determine at the beginning of the method that the elements are grouped in common into a partition. As a result of this development of the method, it becomes possible to assure that, for example given controlled sources, both the controlling elements as well as the controlled source can be processed in common in one partition. This development also makes it possible to likewise allocate connecting leaps in the electrical circuit that only comprise at least one voltage source and/or at least one inductance in common in one partition. This procedure also makes it possible to avoid shorts that may potentially occur due to the partitioning.

Due to the development of the method that a plurality of edges of the graph have a common weighting value allocated to them, the implementation of the method is further accelerated by a computer since, given this

development, a lower number of weighting values must be taken into consideration during the course of the method.

It is also advantageous to form a plurality of partitions for the electrical circuit, to again image the corresponding graphs of the partitions onto the electrical circuit for the partitions, and to process the arising partitions of the electrical circuit in parallel on different computers or, respectively, processors. As a result of this parallelization, a circuit simulation of an extremely large circuit can be implemented significantly faster then given a purely "serial" circuit simulation.

It is also advantageous in the parallelized circuit simulation, to control the processing of the individual partitions centrally. In this way, a controlled circuit simulation is realized with optimally low communication outlay.

It is also advantageous to additionally provide the individual terminals of the partitions that are coupled to components that do not lie in their partition with a voltage source and a resistor, whereby the voltage source has the electrical boundary descriptive quantities respectively allocated to it by a central control unit that controls the parallelized processing of the partitions. As a result of the resistor that is respectively provided in the terminals, the convergence of the circuit simulation is assured during the parallelized circuit simulation, the value thereof being dynamically adapted by the control unit.

The Figures show an exemplary embodiment of the method that is explained in greater detail below.

Shown are:

Fig. 1 a flow chart wherein the individual method steps of the method are shown;

Fig. 2 a sketch that shows various developments of the method.

Electrical circuits that comprise an extremely great plurality of elements can be parallelized into an arbitrary plurality of partitions and a processing of the individual partitions on different computers or, respectively, processors that implement a circuit simulation. The implementation of the overall circuit simulation can thus be considerably speeded up.

In order for the parallelization, however, to be designed as optimally as possible, the individual partitions must be carefully defined.

It is thereby important, first to make sure of an approximately uniform size of the partition and, second, to make sure that the individual partitions do not comprise an excessively great plurality of terminals "toward the outside", for example couplings to other elements not lying in the partition.

Electrical circuits for processing within the framework of a circuit simulation by a computer are usually present in a circuit description language 101, for example in what is referred to as the language SPICE, which is described in the document [1].

The method, however, is definitely not limited to a description of the electrical circuit in a circuit description language and is likewise not limited to the employment of the specific circuit description language SPICE.

In a first method step 102, the electrical circuit is imaged on a graph that exhibits the same topology as the electrical circuit. This ensues, for example, proceeding from the electrical circuit present in the circuit description language SPICE. The graph comprises the corresponding nodes corresponding to the topology of the electrical circuit. The individual elements of the electrical circuit are represented by edges between the nodes of the graph.

It is advantageous in a development of the method to mark individual elements of the electrical circuit at the beginning of the method, i.e. to determine for the corresponding, marked elements that the marked elements are respectively allocated in common to one partition in the further method. Various markings can assign various elements to different partitions. It is also provided to mark elements only in a way that is interpreted such by the computer that implements the method that the respectively paired elements are allocated to one partition.

It is thereby advantageous, for example, to take the following specific instances of an electrical circuit into consideration. When an electrical circuit contains controlled sources, for example controlled current sources or controlled voltage sources, then it is advantageous that both the controlling

elements as well as the controlled source are contained in common in one partition for the later circuit simulation.

It is further advantageous to likewise allocated coupled inductances to a common partition. It is also important to take into consideration in a development of the method that no shorts dare occur due to the partitioning and the algorithmic processing thereof with a computer.

In a further step 103, weighting values G are allocated to the edges. The weighting values G describe what calculating outlay is approximately expected for determining electrical descriptive quantities for the respective element of the electrical circuit that is represented by the edge to which the weighting value G is respectively assigned.

One criterion for the required calculating outlay is to be seen, for example, in the plurality of code lines required for determining the electrical descriptive quantities for the respective, specific element within the framework of the circuit simulation. It should be noted here as a rough rule that the determination of the electrical descriptive quantities for transistors is substantially greater than the outlay for determining the electrical descriptive quantities for an electrical resistor or for a capacitor as well. The selection of the weighting values G, however, is basically uncritical and merely represents an approximate size relationship of the required calculating outlay. It is even adequate to allocate a high weighting value G, for example, the weighting value G = 300 to, for example, an edge that represents a transistor and to allocate a low weighting value, for example a weighting value G =1 or even a weighting value G = 0, to the edges that represent a resistor or a capacitor.

What are to be understood as electrical descriptive quantities in this conjunction are, for example, the corresponding currents and voltages of an element of the electrical circuit.

A first iteration loop implemented thereafter contains the following method steps.

A n arbitrary edge of the graph is selected 104 at the beginning of the first iteration loop. However, it is likewise provided in one version of the

method to select an arbitrary plurality of edges of the graph coupled to one another in this method step, as a result whereof the number of required iterations in the first iteration loop 105, 106, 107 is substantially reduced. Two method steps 106, 107 described later are implemented, proceeding from the selected edge or, respectively, proceeding from the set of selected edges, until the first sum value SW1 is greater than a freely prescribable, first threshold S1.

The first sum value SW1 is formed for respectively at least one new edge that was not contained in the set of considered edges from the last iteration or, respectively, that was not contained in the selected set of edges at the beginning of the first iteration loop. The first sum value SW1 is formed, for example, by summation of the weighting values G of all of the edges that are utilized 106 for the formation of the first sum value SW1.

When the first sum value SW1 is not greater then the first threshold S1, a partition of the electrical circuit derives from the edges that were utilized 107 for the formation of the first sum value SW1, and the method steps of the first iteration loop are re-implemented, now with the "new" partition.

When, however, the first sum value SW1, is greater then the first threshold S1, then the partition formed in the iteration step preceding in time is employed, and method steps of a further, second iteration loop are implemented for the partition that is formed.

Proceeding from the respective partition, the following method steps are implemented 108 in each iteration step of the second iteration loop for at least a part of the remaining edges of the electrical circuit. What is to be understood by a remaining edge in this context is an edge that is not already contained in the partition itself and that is coupled to an edge that is contained in the partition, for example via a node in the partition.

A second sum value SW2 is formed 109 from the weighting values of the partition and the weighting values of at least one additional, remaining edge. This ensues, for example, by simple summation over the weighting values G allocated to the corresponding edges.

A check is now carried out to see whether the second sum value SW2 that has been formed is greater than a freely prescribable, second threshold S2 that is higher than the first threshold S1 110.

When the second sum value SW2 is greater then the second threshold S2, then this means that the partition is larger than a prescribable region that can be tolerated. A tolerance region for the size or, respectively, for the maximum required processing outlay that can be tolerated in the circuit simulation of the respective partition is thus described by the first threshold S1 and by the second threshold S2.

When, thus, the second sum value SW2 is greater than the second threshold S2, then the corresponding edge is not added 111 to the partition.

When, however, the second sum value SW2 is not greater then the second threshold S2, then a further check is carried out for the at least one remaining edge to see whether a plurality of edges that were taken into consideration in the formation of the second sum value SW2 and that are coupled to edges that were not taken into consideration in the formation of the second sum value SW2 is smaller than a plurality of edges of the partition that are coupled 112 to the remaining edges.

As can be seen, this comparison corresponds to the plurality of "section points" of every partition with another partition or, respectively, with another element of the electrical circuit as well that is not contained in a partition or, respectively, with a central control unit described later [sic].

When, as can be seen, the number of terminals for each partition thus becomes greater - by adding the at least one remaining edge - then the plurality of terminals of the partition that already previously existed, then the corresponding edge is not added 113. When, however, the new plurality of terminals has been reduced, then the corresponding, remaining edge is added 114 to the partition. For this case, further, the first sum value SW1 for the next iteration of the second iteration loop is occupied with the value of the second sum value SW2.

The second iteration loop is implemented for an arbitrarily prescribable plurality of remaining edges. It is likewise provided in a

development of the method to simply employ the information as to whether all remaining edges have been taken into consideration in the second iteration loop as abort criterion for the second iteration loop. When this is the case, then the second iteration loop is ended in this development. After abort or, respectively, conclusion of the second iteration loop, the partition that was formed in the last iteration of the second iteration loop is employed 116 as partition of the electrical circuit.

Upon employment of the original description of the electrical circuit, for example in the circuit description language SPICE, the partition is imaged into a syntax to be further-processed for the computer, for example again in the circuit description language SPICE. In this imaging, the information of the respective partition for the respective element of the electrical circuit is taken into consideration, for example, by marking the respective element.

As a result of this back-imaging 201 (see Figure 2), thus, a list with the circuit elements of the electrical circuit as well as with the couplings and the respective indication of the partition to which the respective element was allocated in turn arises for the specific cases of employing the circuit description language SPICE.

It is advantageous in a development of the method to implement this method for an arbitrary number of partitions, i.e. the electrical circuit is sub-divided into an arbitrary plurality of partitions. Given this development, partition-specific lists with the elements of the electrical circuit in the circuit description language SPICE arise 202 according to the plurality of partitions formed. A parallelization of the circuit simulation of the electrical circuit that is advantageous in a development of the method is now achieved in that the electrical descriptive quantities for the elements of the electrical circuit are separately identified for each partition, whereby at least a part of the partitions can be processed in parallel on a plurality of computers and/or processors. This corresponds to a parallelization of the circuit simulation.

It is also provided in a development of the method to allocate a common weighting value to a plurality of edges of the graph. The required calculating outlay is reduced as a result of this procedure.

Methods for parallelized circuit simulation on distributed processors or, respectively, distributed computers are known, for example, from the document [2] and [3]. These can be applied without limitation to the partitions formed by the method.

It is also provided in a development of the method to centrally control the parallel processing of the partitions via a central control unit ZS. This means, for example, that the communication of the individual partitions in the method of the circuit simulation as described in documents [2] and [3], i.e. the communication of data ensues only between the central control unit ZS and the part of the partitions that is centrally controlled.

Figure 2 symbolically shows the parallelized processing by a plurality of SPICE data files SPICE.1, SPICE.2, SPICE.3 through SPICE.N. The individual descriptions of the partitions are contained in these SPICE data files in the circuit description language SPICE.

A circuit simulation is implemented 203 for the respective partition, for example centrally controlled by the central control unit ZS.

It is also provided in a development of the method to additionally allocate a voltage source at least to a part of the terminals of the respective partition that is processed in the framework of the parallelized circuit simulation, a corresponding value being respectively allocated to this additional voltage source by the central control unit ZS in the framework of the known method. In order to assure the convergence of the iterative method from document [2] and [3], it is advantageous to additionally provide a resistor at least at a part of the terminals of the respective partitions, the value of said resistor being dynamically adapted by the control unit ZS.

The following publications were cited within the framework of this document:

[1] I. Hoefer, H. Nielinger, SPICE Analyseprogramm für elektronische Schaltungen, Springer Verlag, Berlin, B, ISBN 3-540-15160-5, pp. 7 through 22, 1985.

[2] U. Wever, Q. Zheng et al, Domain Decomposition Methods for circuit Simulation, Proceedings of the 8th Workshop on Parallel and Distributed Simulation, PADS '94 Edinburgh, Scotland, UK, periodical, pp. 183-186. Juli 1994

[3] U. Wever & Q. Zheng, Parallel Transient Analysis for Circuit Simulation, Proceedings of the 29th Annual Hawaii International Conference on System Sciences, periodical, pp. 442 through 447, 1996

[4] B. Riess et al, Partitioning Very Large Circuits Using Analytical Placement Techniques, Proceedings of the 31st ACM/IEEE Design Automation Conference, pp. 646 through 651, 1994

[5] F. Johannes, Partitioning of VLSI Circuits and Systems, 33rd Design Automation Conference, 3-7 June, Las Vegas, pp. 83-87, 1996

[6] J. Cong et al, A Parallel Bottom-Up Clustering Algorithm with Applications to Circuit Partitioning in VLSI Design, In: 30rd Design Automation Conference, 14-18 June, pp. 755-760, 1993

PATENT CLAIMS

1. Computer-supported method for partitioning an electrical circuit,
- whereby the electrical circuit is imaged onto a graph that exhibits the same topology as the electrical circuit,
- whereby edges of the graph have weighting values allocated to them with which a required calculating outlay for determining electrical descriptive quantities for elements of the electrical circuit that are represented by the respective edge is described,
- whereby a first sum value of the weighting values of the edges is calculated for edges coupled to one another and, in further iterations, the first sum value is respectively formed upon addition of at least one further edge until the respectively calculated, first sum value is greater than a prescribable, first threshold,
- whereby a partition of the electrical circuit is formed by the edges taken into consideration in the formation of the first sum value,
- whereby the following steps are implemented for at least a part of the remaining edges that do not lie in the partition and that are coupled to at least one edge of the partition:
-- a second sum value is determined that derives from the sum of the first sum value and at least one weighting value of at least one remaining edge,
-- when the second sum value is smaller than a prescribable second threshold, and
-- when a plurality of edges that were taken into consideration in the formation of the second sum value that are coupled to edges that were not taken into consideration in the formation of the second sum value is smaller than a plurality of edges of the partition that are coupled to the remaining edges, then
-- the remaining edge is allocated to the partition and the second sum value is allocated to the first sum value, and

- whereby the partition is formed by the edges taken into consideration in the formation of the second sum value.

2. Method according to claim 1, whereby a grouping of elements of the electrical circuit for which it is respectively found that these elements are allocated in common to a partition is implemented at the beginning of the method.

3. Method according to claim 2, whereby at least one of the following rules is applied in the grouping of the elements of the electrical circuit:

- elements of a controlled source, at least a controlling element and the controlled source, are allocated in common to a partition,
- connecting loops in the electrical circuit that only contain at least one voltage source and at least one counter-inductance are allocated in common to a partition,
- no shorts dare arise due to the partitioning.

4. Method according to one of the claims 1 through 3, whereby a plurality of edges of the graph have a common weighting value allocated to them.

5. Method according to one of the claims 1 through 4, whereby the graph of the partition is imaged onto the electrical circuit, whereby the partition comprises the elements of the electrical circuit corresponding to the implemented partitioning.

6. Method according to one of the claims 1 through 5

- whereby a plurality of partitions are formed by multiple implementation of the method, and
- whereby the electrical descriptive quantities for the elements of the electrical circuit are determined for each partition, whereby at least a part of

the partitions is processed in parallel on the plurality of computers and/or processors.

7. Method according to claim 6, whereby the parallel processing of the partitions is centrally controlled.

8. Method according to claim 7, whereby at least a part of the partitions are centrally controlled in such a way that all terminals of the respective partition are coupled only to a central control unit and, thus, a communication of data ensues only between the central control unit and at least the part of the partitions.

9. Method according to claim 8, whereby a voltage source is additionally allocated at least to a part of the terminals of the respective partition, the value of said additional voltage source to be predetermined by the central control unit during the determination of the electrical descriptive quantities.

10. Method according to claim 9, whereby a resistor is additionally allocated at least to a part of the terminals of the respective partition.

ABSTRACT

Computer-Supported Method For Partitioning An Electrical Circuit

A partition of an electrical circuit is formed in that the electrical circuit is imaged on a graph (102) and weighting values are allocated (103) to the edges of the graph. The weighting values describe a required calculating outlay for determining electrical descriptive quantities for the respective element of the electrical circuit represented by the edge. A check is carried in iterative methods to see whether, proceeding from preceding iteration steps edges grouped together [sic], [...] a sum of the weighting values of the edges [...] a sum value lies between a first threshold and a second threshold by adding a further edge. When this is the case, then a further check is carried out to see whether a plurality of terminals of the elements within the partition to elements outside the partition is increased by adding new edges. When this is not the case, then the respective edge is also incorporated into the partition.

Fig. 1

EXPRESS MAIL #EL294310959US
BOX PCT

IN THE UNITED STATES ELECTED OFFICE
OF THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY - CHAPTER II

APPLICANT: Utz Wever, et al. ATTORNEY DOCKET NO. P99,0886

SERIAL NO. GROUP ART UNIT:

FILING DATE: EXAMINER:

INTERNATIONAL APPLICATION NO. PCT/DE97/02600

INTERNATIONAL FILING DATE: November 11, 1997

INVENTION: "COMPUTER-SUPPORTED METHOD FOR PARTITIONING AN ELECTRICAL CIRCUIT"

SUBMISSION OF DRAWINGS

Hon. Commissioner of Patents
Washington, D.C. 20231

S I R:

Applicant hereby submits two (2) sheets of drawings for the above-identified application.

Respectfully submitted,

Steven H. Noll, Reg. No. 28,982

Steven H. Noll
HILL & SIMPSON
A Professional Corporation
85th Floor - Sears Tower
Chicago, Illinois 60606
Telephone (312) 876-0200

Attorneys for Applicant

FIG 1

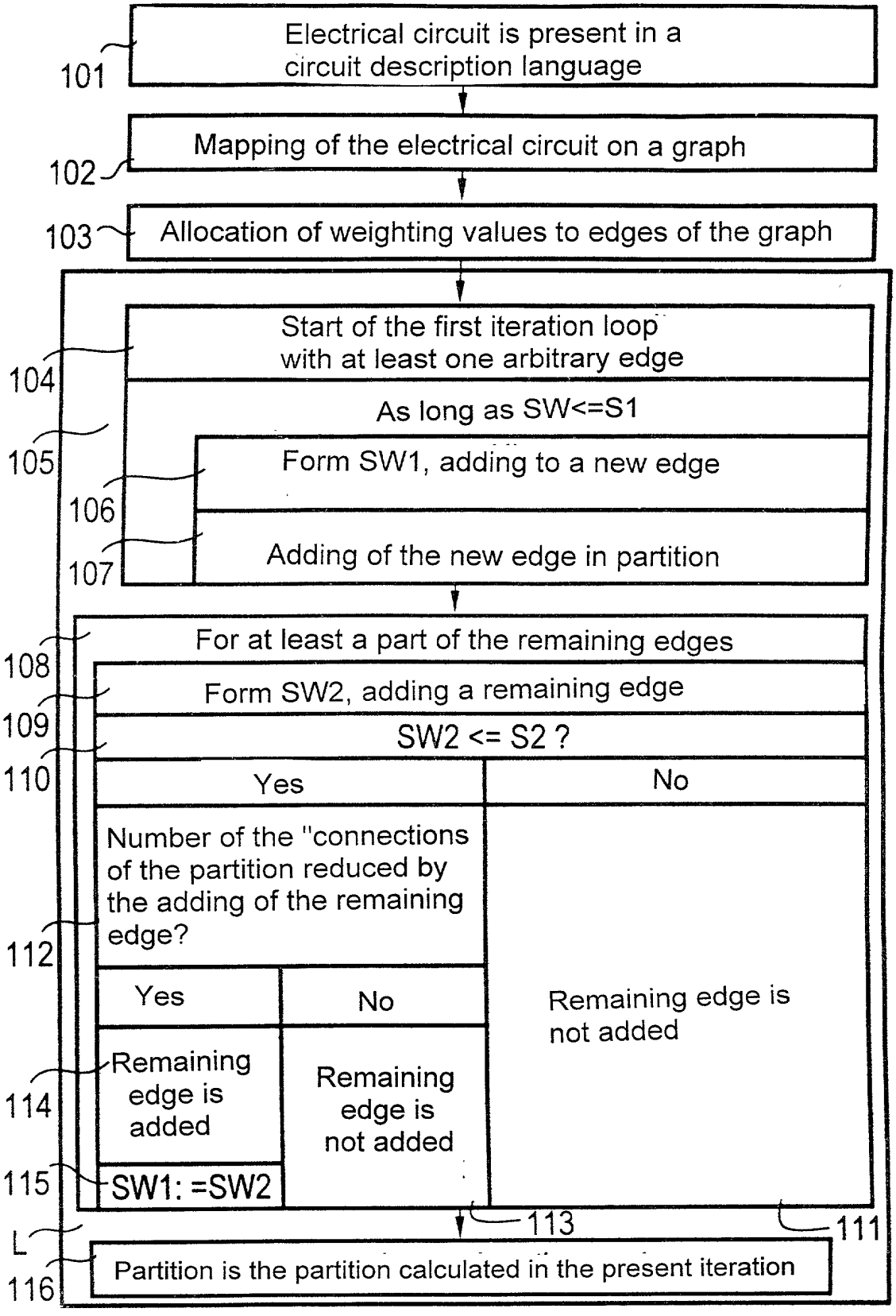
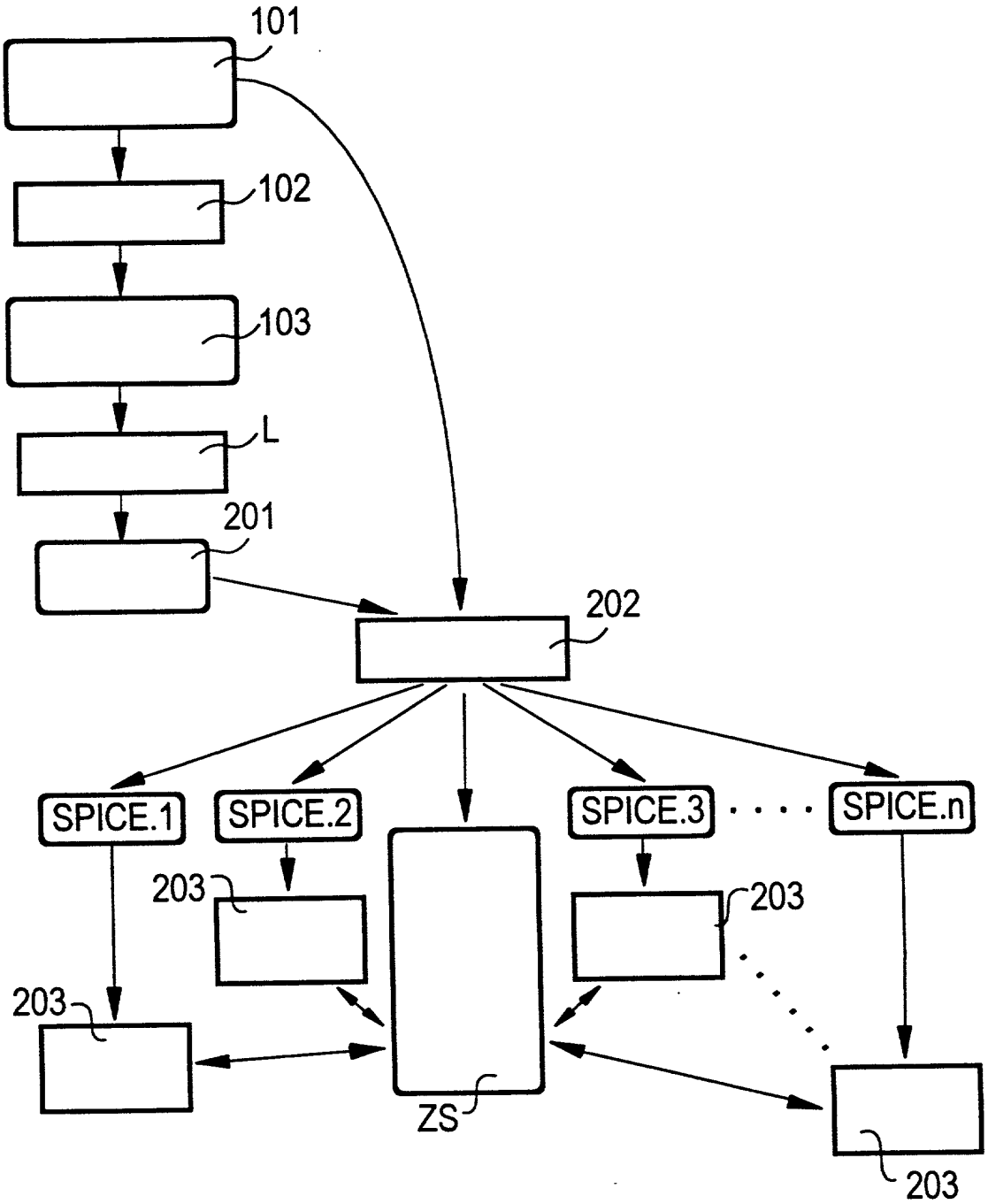

Electrical circuit is present in a circuit description language
101
Mapping of the electrical circuit on a graph
102
Allocation of weighting values to edges of the graph
103
Start of the first iteration loop with at least one arbitrary edge
104
As long as SW<=S1
105
Form SW1, adding to a new edge
106
Adding of the new edge in partition
107
For at least a part of the remaining edges
108
Form SW2, adding a remaining edge
109
SW2 <= S2 ?
110
Yes
No
Number of the "connections of the partition reduced by the adding of the remaining edge?
112
Yes
No
Remaining edge is not added
Remaining edge is added
114
Remaining edge is not added
SW1: =SW2
115
113
111
L
Partition is the partition calculated in the present iteration
116

FIG 2


101
102
103
L
201
202
SPICE.1
SPICE.2
SPICE.3
SPICE.n
203
203
203
ZS
203

Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

As a below named inventor, I hereby declare that:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

My residence, post office address and citizenship are as stated below next to my name,

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent beantragt wird für die Erfindung mit dem Titel:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

Rechnergestütztes Verfahren zur Partitionierung einer elektrischen Schaltung

deren Beschreibung

(zutreffendes ankreuzen)

☒ hier beigefügt ist.

☐ am _____ als PCT internationale Anmeldung PCT Anmeldungsnummer _____ eingereicht wurde und am _____ abgeändert wurde (falls tatsächlich abgeändert).

the specification of which

(check one)

☐ is attached hereto.

☐ was filed on _____ as PCT international application PCT Application No. _____ and was amended on _____ (if applicable)

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

German Language Declaration

Prior foreign appplications
Priorität beansprucht

			Priority Claimed	
196 47 622.4	Germany	18. November 1996	☒	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein
			☐	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein
			☐	☐
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)	Yes Ja	No Nein

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Serial No.) (Anmeldeseriennummer)	(Filing Date) (Anmeldedatum)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date) (Anmeldedatum)	(Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

Ich erkläre hiermit, dass alle von mir in der vorliegenden Erklärung gemachten Angaben nach meinem besten Wissen und Gewissen der vollen Wahrheit entsprechen, und dass ich diese eidesstattliche Erklärung in Kenntnis dessen abgebe, dass wissentlich und vorsätzlich falsche Angaben gemäss Paragraph 1001, Absatz 18 der Zivilprozessordnung der Vereinigten Staaten von Amerika mit Geldstrafe belegt und/oder Gefängnis bestraft werden koennen, und dass derartig wissentlich und vorsätzlich falsche Angaben die Gültigkeit der vorliegenden Patentanmeldung oder eines darauf erteilten Patentes gefährden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

German Language Declaration

VERTRETUNGSVOLLMACHT: Als benannter Erfinder beauftrage ich hiermit den nachstehend benannten Patentanwalt (oder die nachstehend benannten Patentanwälte) und/oder Patent-Agenten mit der Verfolgung der vorliegenden Patentanmeldung sowie mit der Abwicklung aller damit verbundenen Geschäfte vor dem Patent- und Warenzeichenamt: *(Name und Registrationsnummer anführen)*

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

And I hereby appoint

Messrs. John D. Simpson (Registration No. 19,842) Lewis T. Steadman (17,074), William C. Stueber (16,453), P. Phillips Connor (19,259), Dennis A. Gross (24,418), Marvin Moody (16,549), Steven H. Noll (28,982), Brett A. Valiquet (27,841), Thomas I. Ross (29,275), Kevin W. Guynn (29,927), Edward A. Lehmann (22,312), James D. Hobart (24,149), Robert M. Barrett (30,142), James Van Santen (16,584), J. Arthur Gross (13,615), Richard J. Schwarz (13,472) and Melvin A. Robinson (31,870), David R. Metzger (32,919), John R. Garrett (27,888) all members of the firm of Hill, Steadman & Simpson, A Professional Corporation.

19

Telefongespräche bitte richten an: *(Name und Telefonnummer)*

Direct Telephone Calls to: *(name and telephone number)*

312/876-0200
Ext. _____

Postanschrift:

Send Correspondence to:

HILL, STEADMAN & SIMPSON
A Professional Corporation
85th Floor Sears Tower, Chicago, Illinois 60606

Voller Name des einzigen oder ursprünglichen Erfinders: WEVER, Utz	Full name of sole or first inventor:
Unterschrift des Erfinders Datum 30.10.97	Inventor's signature Date
Wohnsitz D-81539 München, Germany DEX	Residence
Staatsangehörigkeit Bundesrepublik Deutschland	Citizenship
Postanschrift Herzogstandstr. 28 81539 München Bundesrepublik Deutschland	Post Office Addess
Voller Name des zweiten Miterfinders (falls zutreffend): ZHENG, Qinghua	Full name of second joint inventor, if any:
Unterschrift des Erfinders Datum 30.10.97	Second Inventor's signature Date
Wohnsitz D-82024 Taufkirchen, Germany DEX	Residence
Staatsangehörigkeit Bundesrepublik Deutschland	Citizenship
Postanschrift Sudetenstr. 51 D-82024 Taufkirchen Bundesrepublik Deutschland	Post Office Address

(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors).